



S J P N Trust's

Hirasugar Institute of Technology, Nidasoshi.*Inculcating Values, Promoting Prosperity*

Approved by AICTE, New Delhi, Permanently Affiliated to VTU, Belagavi

Recognized under 2(f) & 12B of UGC Act, 1956

Accredited at 'A' Grade by NAAC & Programmes Accredited by NBA: CSE & ECE

EEE Dept.

EESSA

Activity Report

2022-23
(Odd Sem)**DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGG.**

Date of Activity held	18/11/2022
Time	12.00 noon to 01.00 pm
Type of Activity (Co-curricular)	Technical Talk on “Analog & Digital IC Design Flow”
Resource Person:	Shri. Gangadhar Naik
Professional Details of Resource Persons/Guests	Senior Staff Manager, Marvel Semiconductor, Bangalore.
Year / Class –	All Students
No. of students-	61
Activity In charge-	Prof. M. P. Yenagimath

Description of Activity:

EESSA organized a technical talk on the topic “**Analog & Digital IC Design flow**” on 18th November 2022 at 12:00 noon for the students of Electrical and Electronics Engineering department.

Prof. M. P. Yenagimath, EESSA Staff Coordinator welcomed the gathering and introduced the resource person.

The resource person Shri. Gangadhar Naik, Senior Staff Manager, Marvel Semiconductor, Bangalore discussed about various aspects of Analog and Digital IC design. Also highlighted about Analog ASIC design with product specification, circuit design, and architecture. And at the end, interacted with final year students and discussed about the job opportunities in VLSI Industries.

The technical talk concluded with feedback from students and presidential remarks by Dr. B. V. Madiggond, HOD, EEE.



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Activity Photographs: Technical Talk on “Analog & Digital IC Design Flow”

